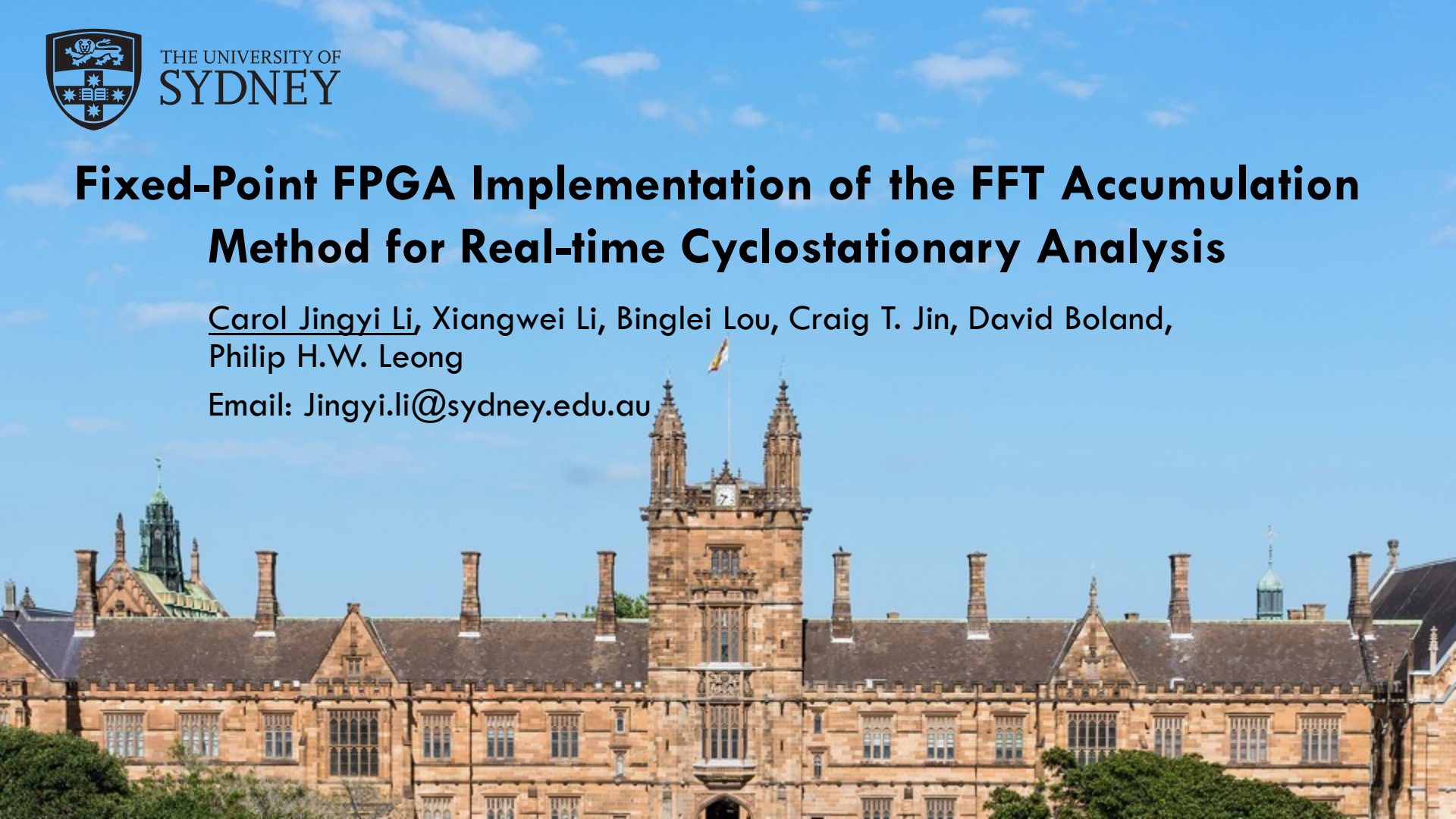

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Fixed-Point FPGA Implementation of the FFT Accumulation Method for Real-time Cyclostationary Analysis

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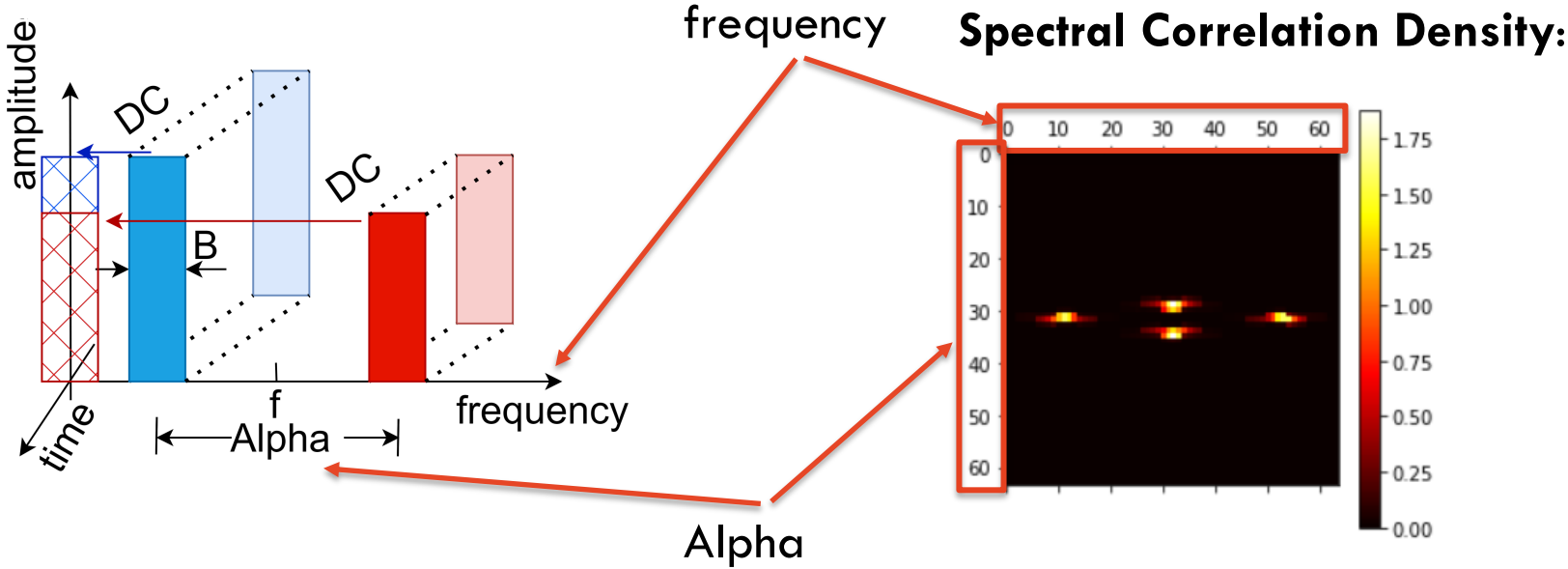
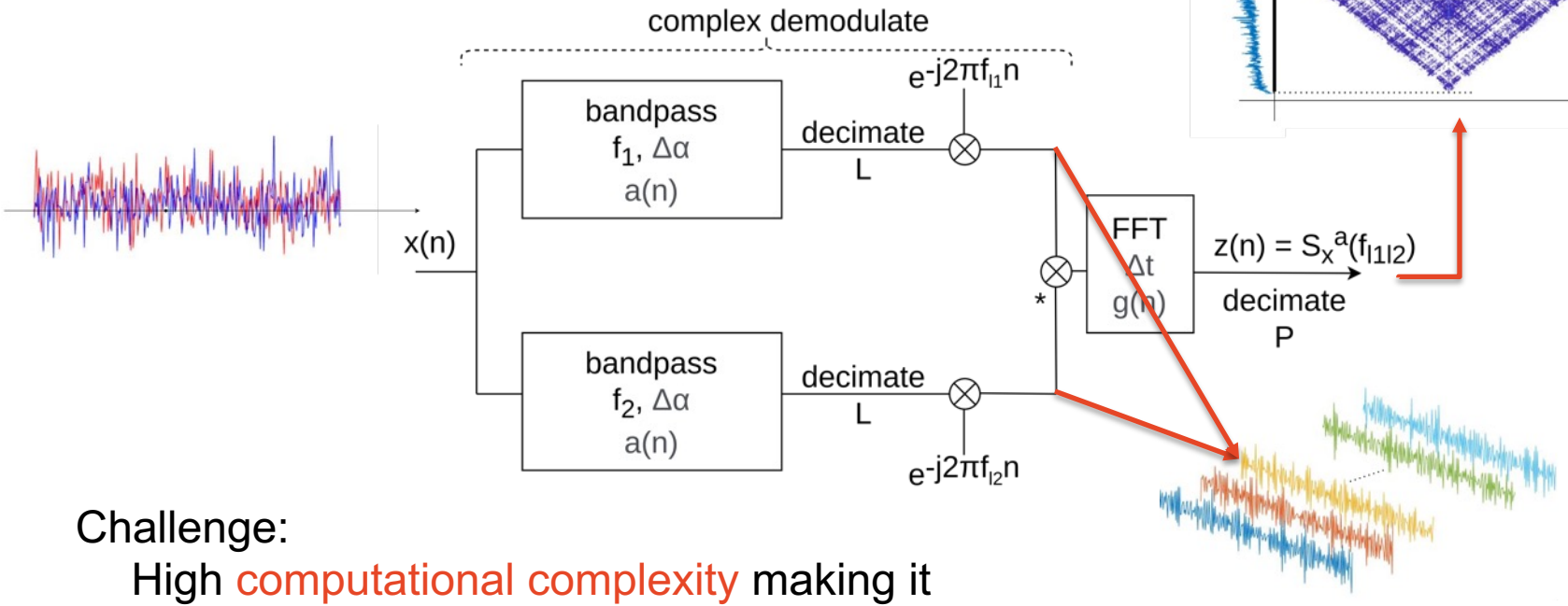
Introduction

A time series is said to be **cyclostationary** if its probability distribution varies periodically with time.



Spectral Correlation Density (SCD)

FFT Accumulation Method (FAM)



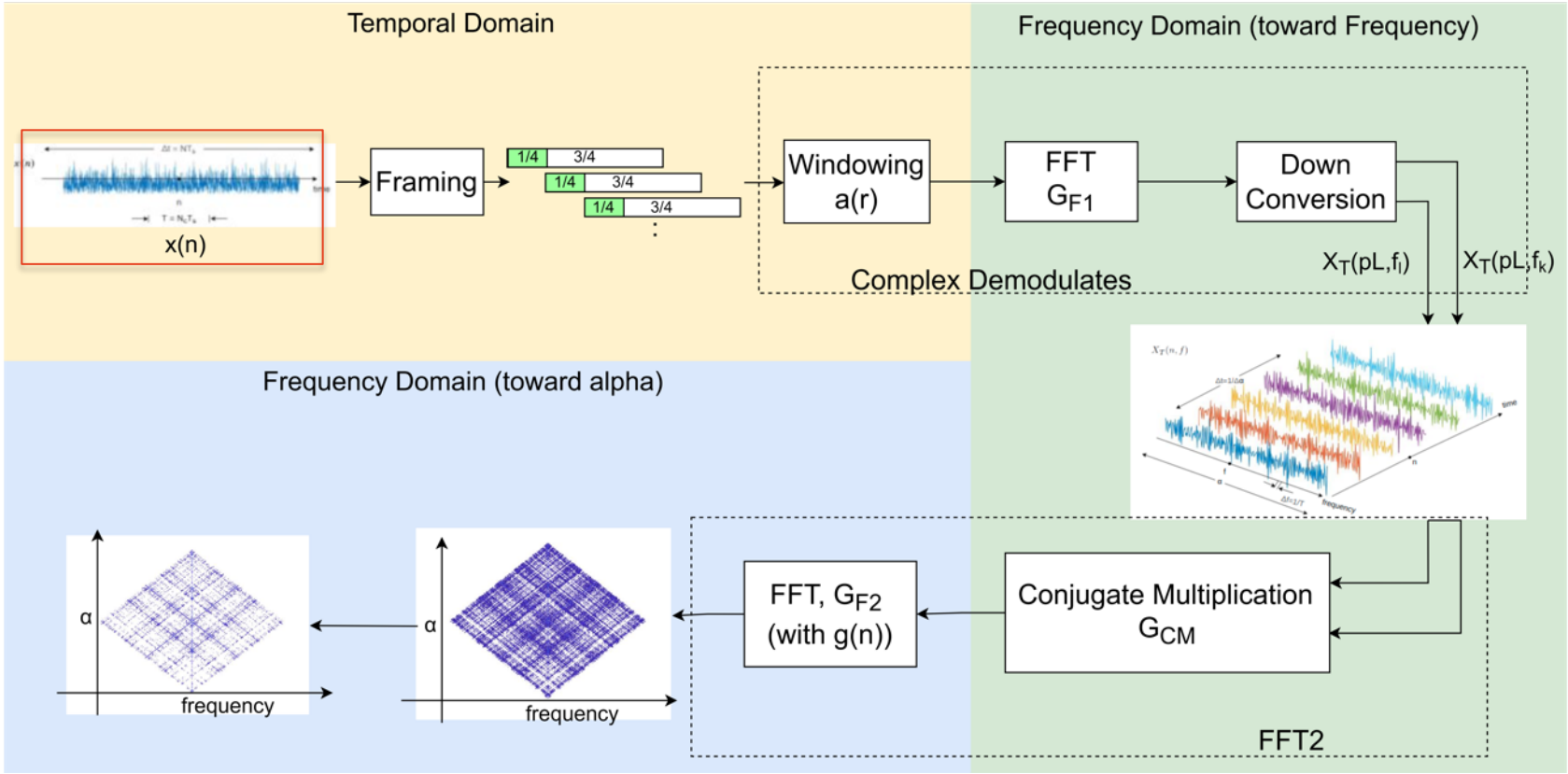
Challenge:

High computational complexity making it difficult to use in real-time applications.

Contribution

- The first analytical SQNR model.
  - Fixed-point implementations of the **FAM** technique.
  - Tradeoffs between **precision** and **area**.
- A quantitative comparison of two wordlength assignment strategies.
  - FAM_M1 - fixed wordlength
  - FAM_M2 - mixed precision
- A highly parallel architecture.
  - **Minimises** resource usage through precision optimization.
  - HLS implementation achieves the **best** reported throughput and **lowest** power consumption.

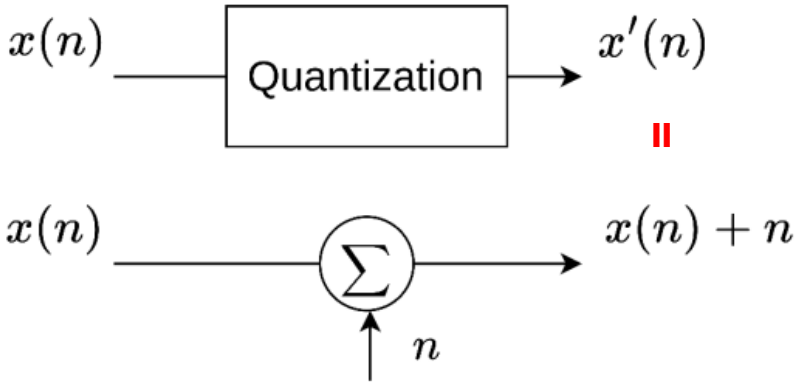
SCD Signal Flow Graph



Quantization noise model

Fixed-point: $a = -a_{B-1} + \sum_{i=0}^{B-2} a_i, 2^{i-(B-1)}$

Range: [-1,1)
B: wordlength
F: fractional bits (F = B-1)



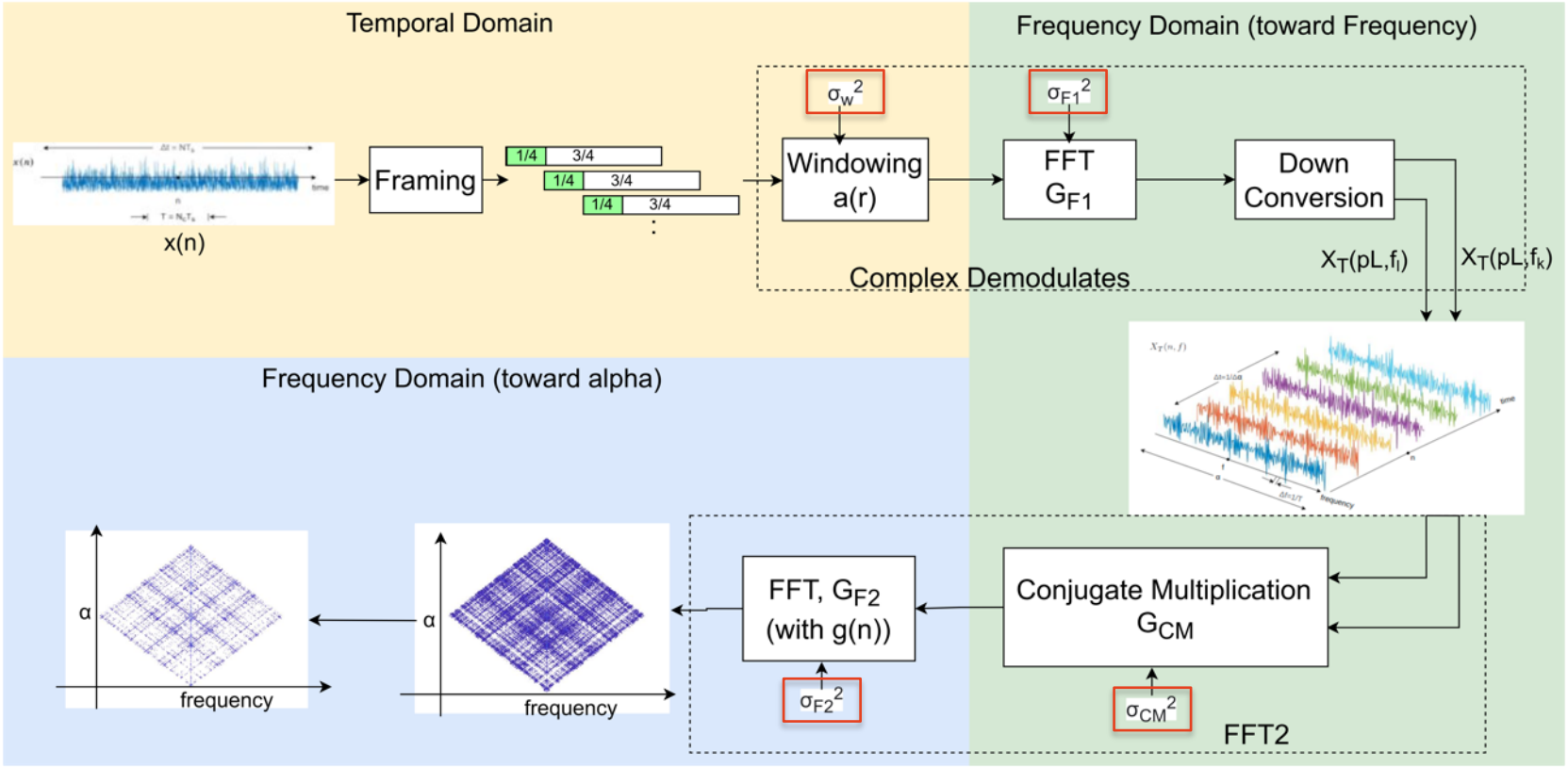
Rounding Error

$$\sigma_m^2 = \frac{(2^{-F})^2}{12}$$

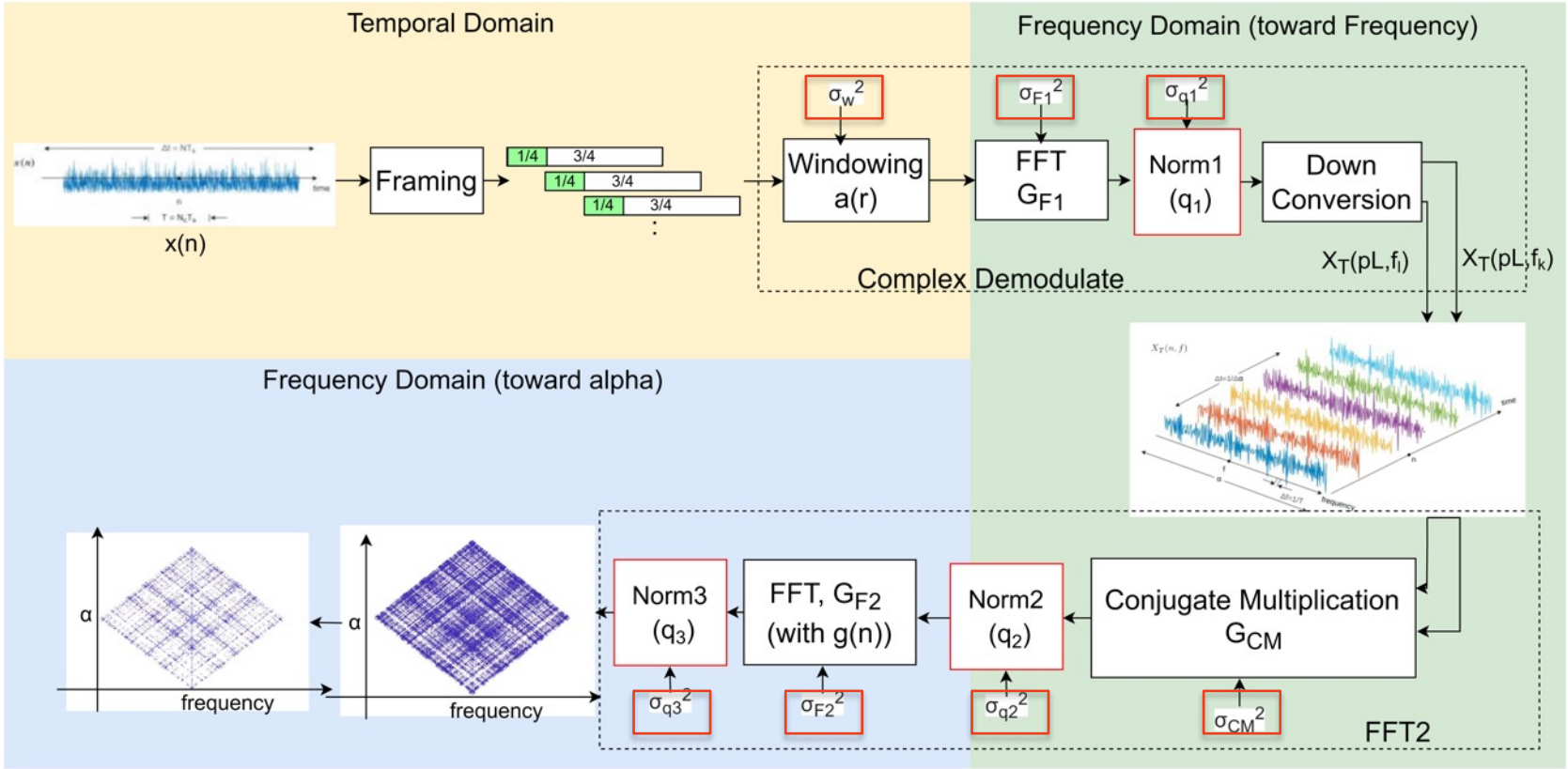
Truncation Error

$$\sigma_{ad}^2 = \frac{(2^{-F})^2}{8}$$

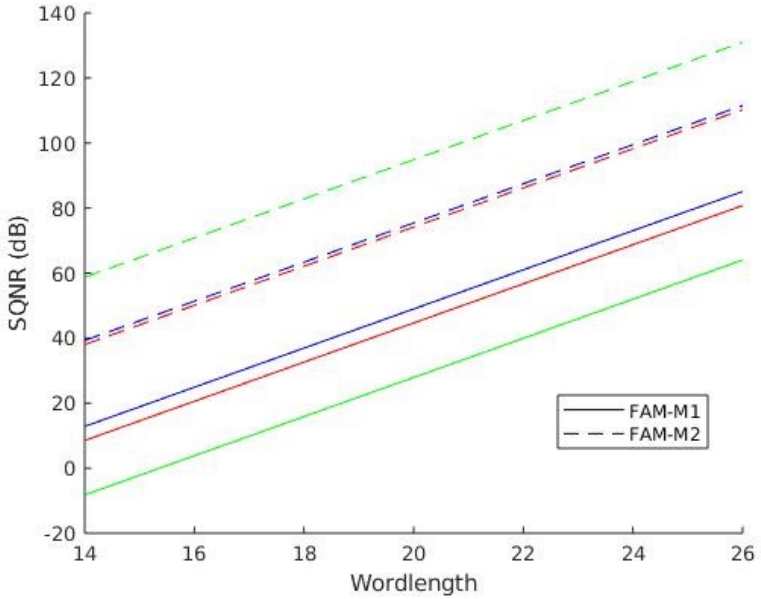
SCD Signal Flow Graph for FAM_M1 (Fixed)



SCD Signal Flow Graph for FAM_M2 (Mixed)

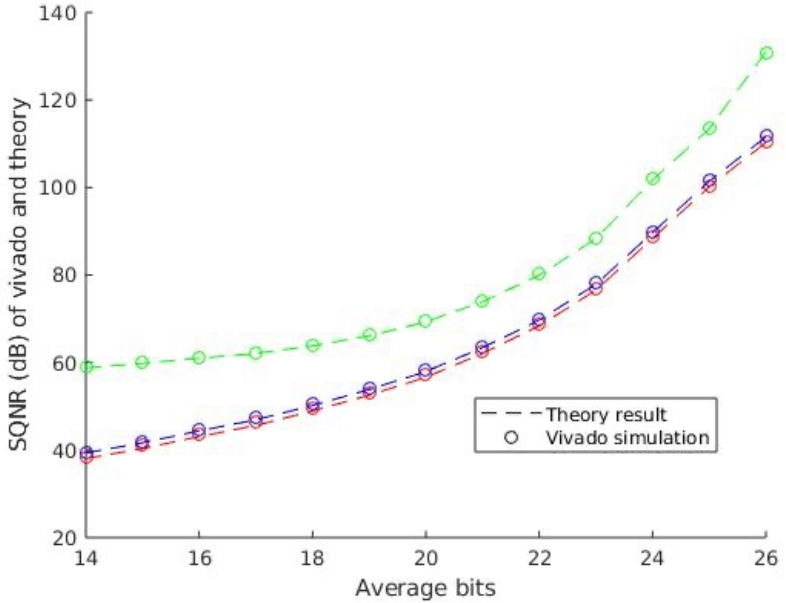


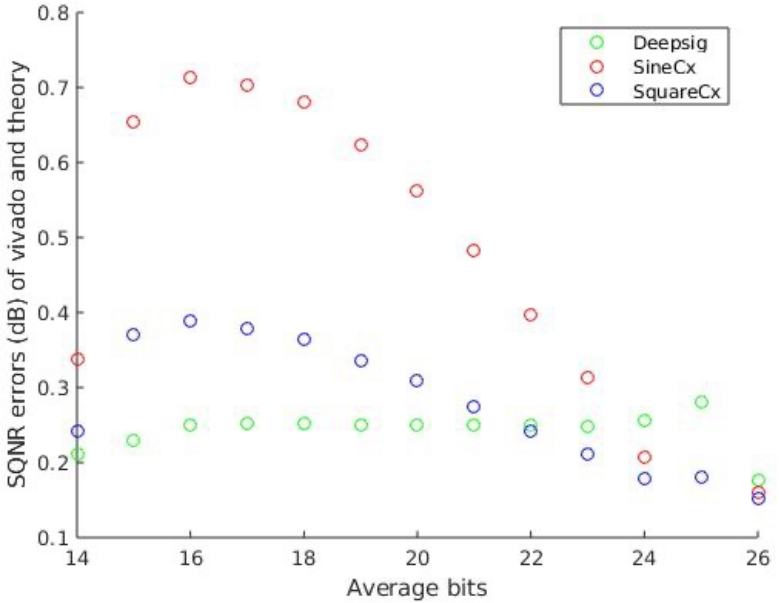
Quantization Error Analysis



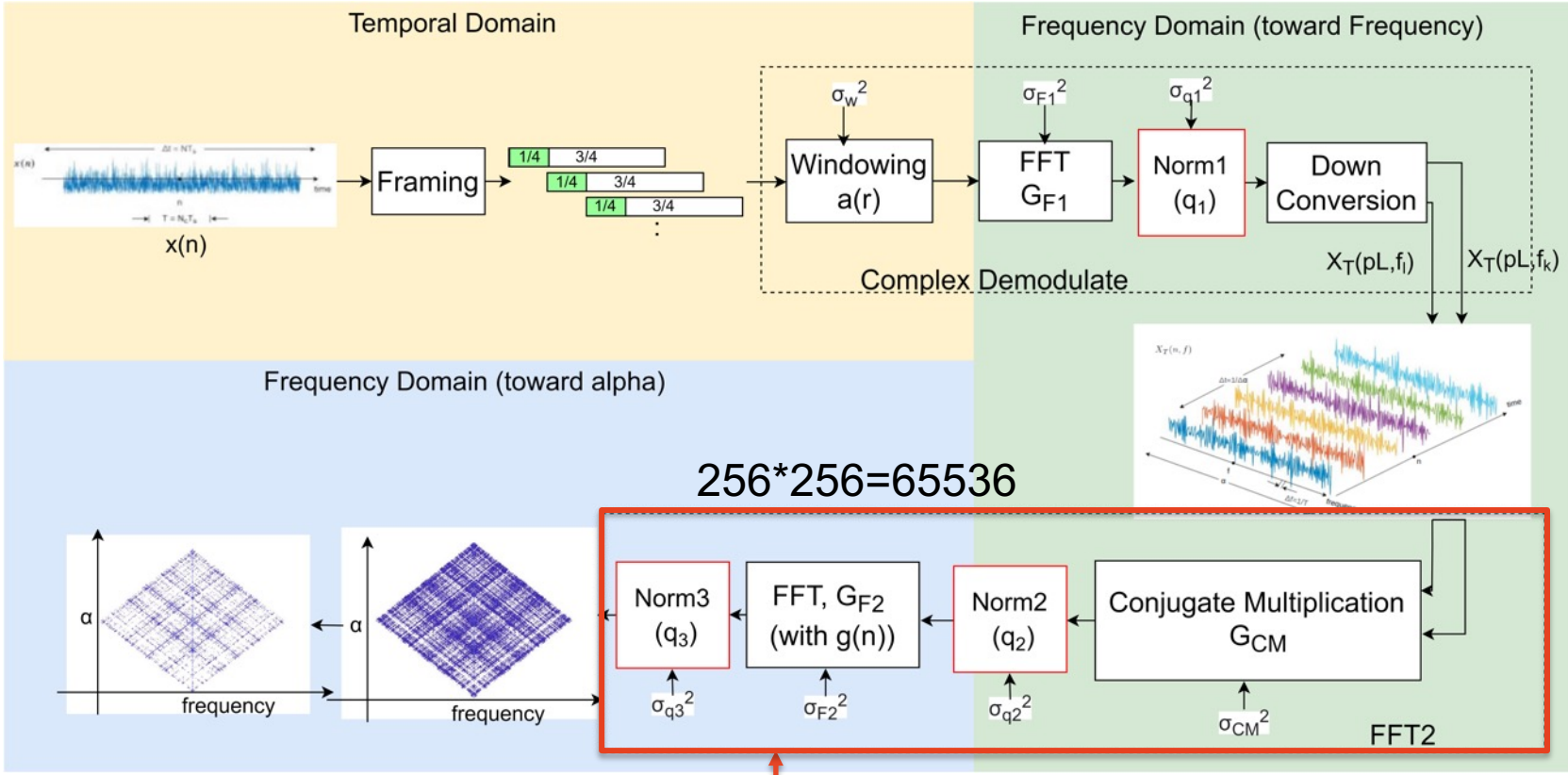
- **FAM_M1**
  - Requires rescaling after additions to avoid overflow
- **FAM_M2**
  - Higher SQNR
  - Uses longer wordlengths

Quantization Error Analysis for FAM_M2

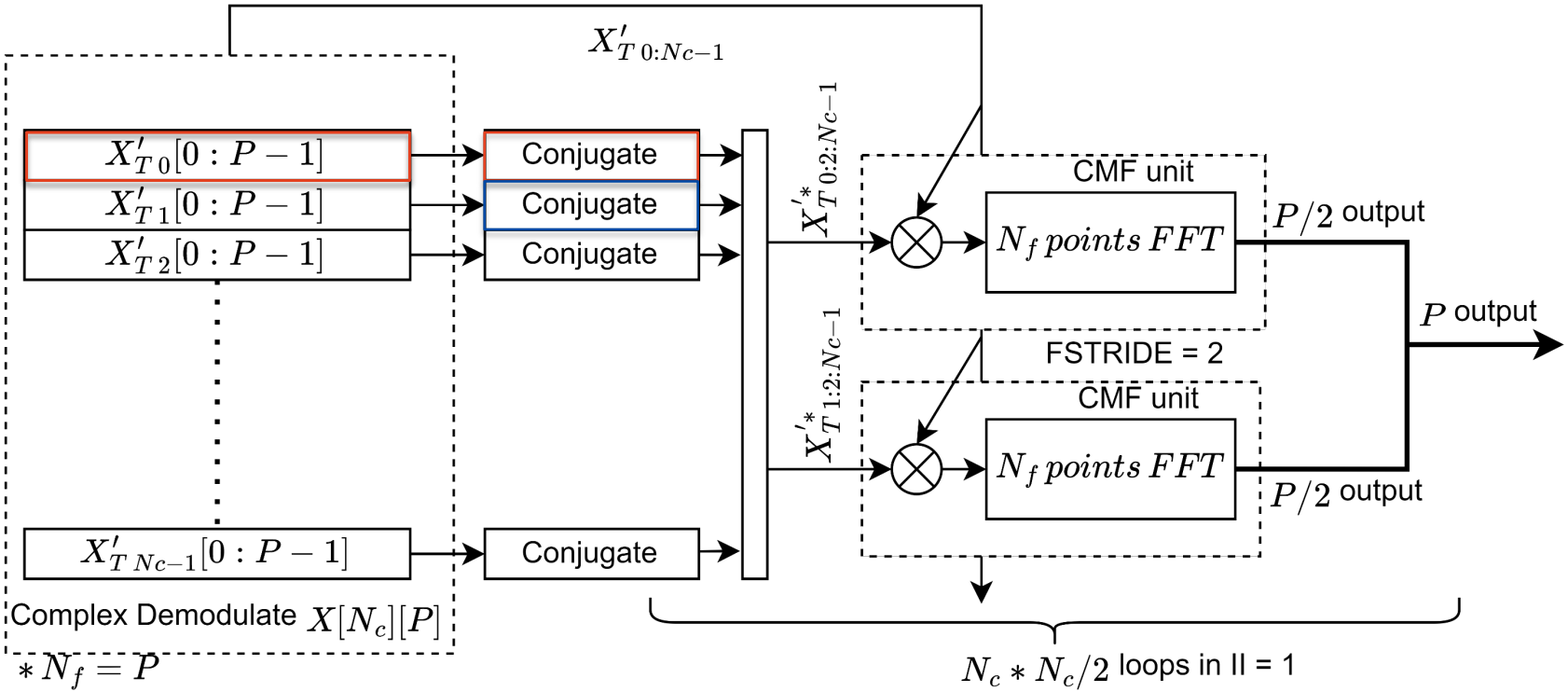




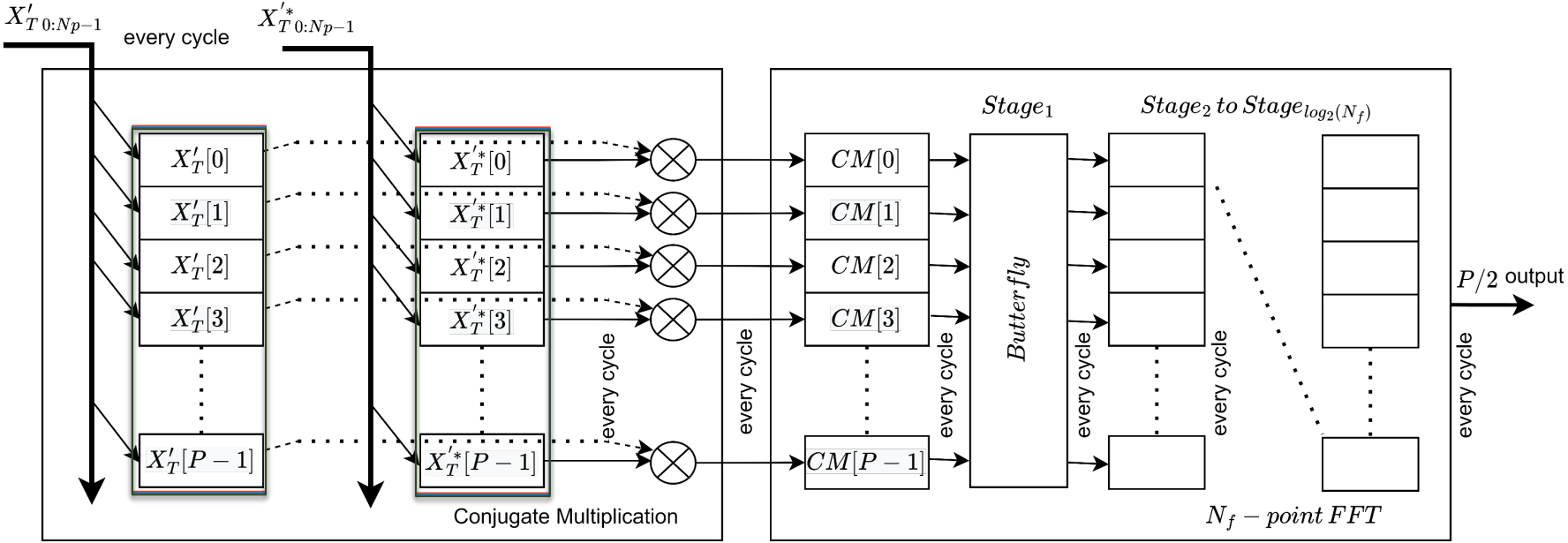
SCD Signal Flow Graph for FAM_M2



FSTRIDE in FFT2

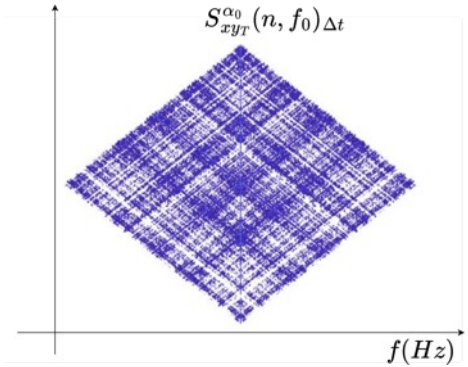


Pipelining the CMF unit



Sparse SCD matrix output

- **To minimise accelerator-to-host bandwidth**

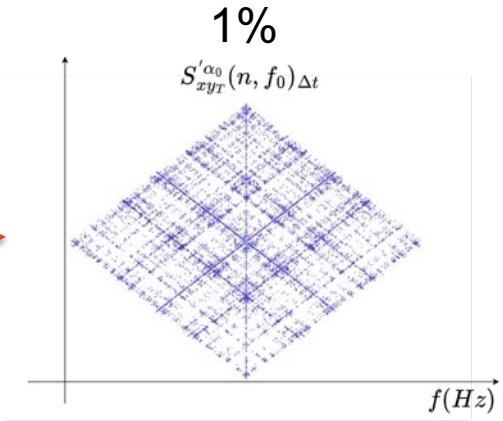


Value > threshold

Frequency Label

Alpha Label

1%

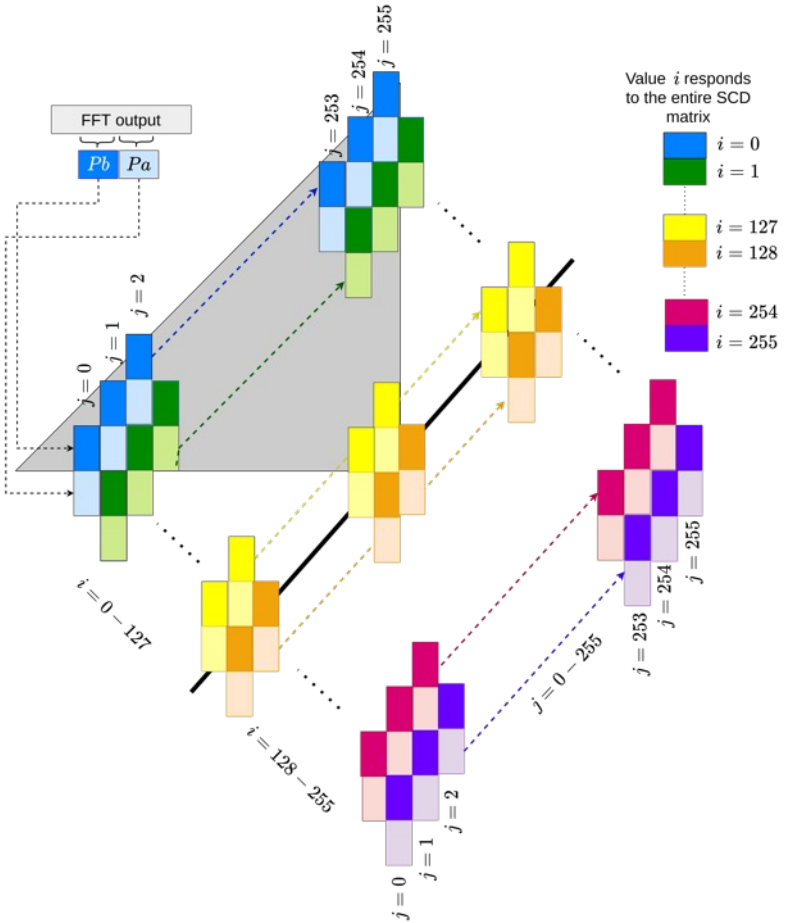


Symmetry

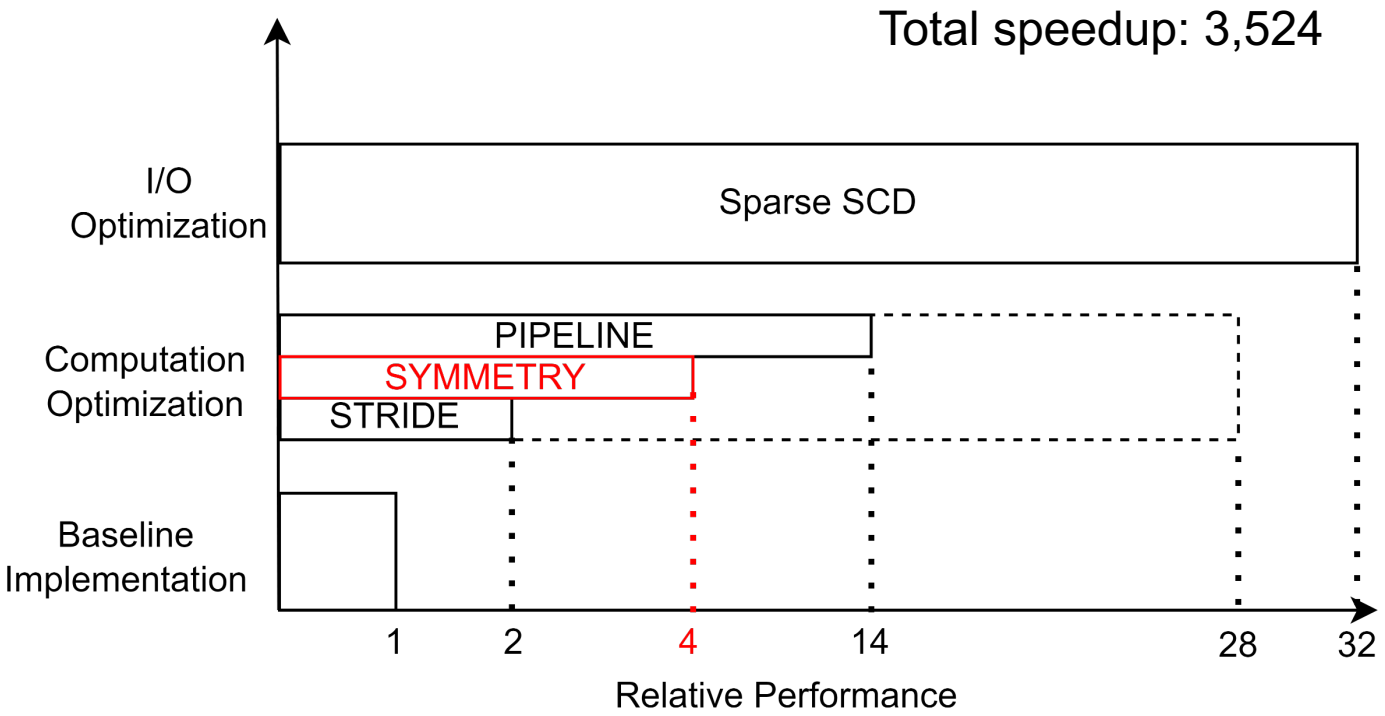
- **Quarter SCD matrix**

$$\hat{S}_x^{\alpha}(f) = \hat{S}_x^{\alpha}(-f)$$

$$\hat{S}_x^{-\alpha}(f) = \hat{S}_x^{\alpha}(f)^*$$



Optimisation breakdown



Resource Utilization for FAM_M2 (Quarter)

	WL	LUTs	DSPs	FFs	BRAMs	SQNR	Fmax (MHz)
Percentage of XCZU28DR	16	23.0%	24.5%	10.5%	16.4%	71.05	200
Resources	--	425,280	4,272	850,560	1,080	--	--

Comparison with Previous Works

Platform	Throughput (MS/s)	Energy (mJ)	Power (W)
Tegra K1 [1]	0.018	390.64	3.5
Tesla K20 [1]	0.228	457.98	51
ZedBoard+TegraK1[1]	0.04	254.75	5
Tesla K40 [2]	6.8	16.817	55.5
ZCU111[3]	31.5	0.8125	12.5
ZCU111Opt_Quarter	50	0.3116	7.6

[1] N. Bidyanta et al., "**GPU and FPGA based architecture design for real-time signal classification**", 2015
[2] S. Marshall et al., "**GPGPU based parallel implementation of spectral correlation density function**", 2020
[3] Xiangwei Li et al., "**A Scalable Systolic Accelerator for Estimation of the Spectral Correlation Density Function and Its FPGA Implementation**", 2022

Conclusion

- **Optimised implementation of the FAM technique**
  - Analytic Quantization Error Analysis
  - Mixed-precision model has much better SQNR than fixed wordlength
  - Presented architecture which exploited Spatial Parallelism, Pipelining, I/O optimization, and Symmetry to achieve high throughput and energy consumption to achieve a > 3000x speedup over serial implementation
- Future work: use this as preprocessing for real-time cyclostationary applications

Questions?

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